REMARKS

Claims 1-33 remain in the application for consideration of the Examiner.

Reconsideration and withdrawal of the outstanding objections are respectfully requested in light of the above amendments and following remarks.

The Examiner requests formal drawings.

By separate letter, Applicants have submitted formal drawings in accordance with the Examiner's request.

Claims 12-15, 25, 26, and 33 were rejected under 37 CFR 1.75(c) as being of improper dependent form.

The Examiner requires Applicant to cancel the claims, amend the claims, or place the claims in proper dependent form or rewrite the claims in independent forms.

By the instant amendment, Claims 12, 13, 25, 26, and 33 have been rewritten in independent form.

It is respectfully submitted that Claims 12-15, 25, 26, and 33 are of proper dependent form.

Applicants appreciate the indication that Claims 1-11, 16-24, and 27-32 are allowed.

Furthermore, Applicants appreciate the indication that Claims 12-15, 25, 26, and 33 would be allowed if amended to overcome the rejections.

It is respectfully submitted that Claims 12, 13, 25, 26, and 33 have been amended to overcome the objection of the Examiner and consequently it is respectfully submitted that Claims 12-15, 25, 26, and 33 are allowable.

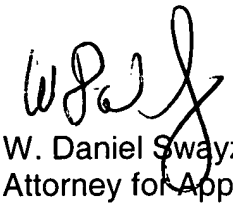
In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 12, 13, 25, 26, and 33 have been amended as follows:

12. A system for extracting a threshold voltage, comprising:

a first MOSFET stage including an input operative to receive a first input current, and a gate node electrically coupled to the input thereof;

a second MOSFET stage including an input operative to receive a second input current and a gate node;

a voltage divider coupled between the input of the second MOSFET stage and the gate node of the first MOSFET stage, the voltage divider also having an intermediate output node coupled to the gate node of the second MOSFET stage, such that an output voltage at the input of the second MOSFET stage is approximately equal to the threshold voltage for at least one of the first and second MOSFET stages; and

~~The system of claim 1 defining a first system for extracting a threshold voltage, further comprising~~ a second system for extracting a threshold voltage coupled to the first system for extracting a threshold voltage to provide a stacked threshold voltage extraction system having an output that is an integer multiple of the threshold voltage of the second system.

13. A system for extracting a threshold voltage, comprising:

a first MOSFET stage including an input operative to receive a first input current, and a gate node electrically coupled to the input thereof;

a second MOSFET stage including an input operative to receive a second input current and a gate node;

a voltage divider coupled between the input of the second MOSFET stage and the gate node of the first MOSFET stage, the voltage divider also having an intermediate output node coupled to the gate node of the second MOSFET stage, such that an output voltage at the input of the second MOSFET stage is approximately equal to the threshold voltage for at least one of the first and second MOSFET stages; and

~~The system of claim 1 in combination with~~ a capacitor multiplier system, the combination comprising:

the capacitor multiplier including a first input that receives the output voltage at the input of the second MOSFET stage and a second input that receives a bias current, such that a startup offset for the capacitor multiplier is mitigated when the bias current is applied to the second input.

25. A system for extracting a threshold voltage, comprising:

a first MOSFET having a drain connected to receive a first input current, a gate electrically coupled to the drain, and a source coupled to a reference potential;

a second MOSFET having a gate, source and drain, the drain being connected to receive a second input current, the source being coupled to the reference potential;

a first part of a voltage divider being coupled between the gate of the first MOSFET and the gate of the second MOSFET;

a second part of the voltage divider being coupled between the gate and the drain of the second MOSFET, such that an output voltage at drain of the second MOSFET is approximately equal to the threshold voltage for at least one of the first and second MOSFETs; and

~~The system of claim 16 defining a first system for extracting a threshold voltage and further comprising~~ a second system for extracting a threshold voltage coupled to the first system for extracting a threshold voltage to provide a stacked threshold voltage extraction system having an output that approximates an integer multiple of the threshold voltage of the second system.

26. A system for extracting a threshold voltage, comprising:

a first MOSFET having a drain connected to receive a first input current, a gate electrically coupled to the drain, and a source coupled to a reference potential;

a second MOSFET having a gate, source and drain, the drain being connected to receive a second input current, the source being coupled to the reference potential;

a first part of a voltage divider being coupled between the gate of the first MOSFET and the gate of the second MOSFET;

a second part of the voltage divider being coupled between the gate and the drain of the second MOSFET, such that an output voltage at drain of the second MOSFET is approximately equal to the threshold voltage for at least one of the first and second MOSFETs;

~~The system of claim 16 in combination with~~ a capacitor multiplier circuit; ~~, the combination comprising:~~

the capacitor multiplier circuit comprising first and second amplifier stages coupled together at a common node, the first stage having a first input that receives a bias current; and

the output voltage from the threshold voltage extraction system being applied to the capacitor multiplier circuit so that voltage approximately equal to the threshold voltage is at the common node, such that a startup offset for the capacitor multiplier circuit is mitigated as the bias current is applied to the first input of the capacitor multiplier circuit.

33. A method for extracting a threshold voltage for a MOSFET device having a gate, source and drain, the method comprising:

connecting gates of first and second stages through a first part of a voltage divider, each stage including a respective MOSFET device;

saturating the MOSFET device of the first stage;

providing bias current to an input of the first stage;

providing bias current to an input of the second stage, the input of the second stage being connected to the gate of the second stage through a second part of the voltage divider;

saturating the MOSFET device of the second stage, such that a voltage at the input of the second stage corresponds to the threshold voltage;

wherein the bias current to the input of the first stage is proportional to the bias current to the input of the second stage; and

~~The method of claim 32, further comprising~~ providing the voltage at the input of the second stage to an input of a capacitor multiplier, such that the threshold voltage is

applied to an internal node of the capacitor multiplier and a startup offset of the capacitor multiplier is mitigated.